Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the applications. Please amend claims 19, 22, and 28-31 as shown below, cancel claims 1-18, 20, 21, 23-27, and 34-41, and add claims 42-52, all without prejudice.

Listing of Claims:

Claims 1-18: Cancelled

2 1

~~19~~.(Presently Amended) The memory system according to claim ~~18~~ ~~33~~, wherein the corresponding sectors in each memory group is calculated in real time.

Claims 20 and 21: Cancelled

3 1

~~22~~.(Presently Amended) The memory system according to claim ~~18~~ ~~33~~, wherein said memory system is a flash memory.

Claims 23-27: Cancelled

4 1

~~28~~.(Presently Amended) The memory system according to claim ~~18~~ ~~33~~, wherein said sector tags and said group tags are settable by a host to which the memory system is connected.

5 4

~~29~~.(Previously Presented) The memory system according to Claim ~~28~~, wherein said sector tags and said group tags are set in response to a host command.

6 5

~~30~~.(Previously Presented) The memory system according to Claim ~~29~~, wherein set ones of said sector tags and said group tags are deselected in response to a host command.

7 1

~~31~~.(Presently Amended) The memory system according to claim ~~18~~ ~~33~~, wherein the number of memory sectors in each memory group is configurable by a host to which the memory system is connected.

Claim 32: Cancelled

33.(Previously Presented) A memory system, comprising:

a plurality of memory groups, each of said memory groups comprising a plurality of memory sectors, each of said memory sectors comprising a plurality of memory cells, wherein the number of memory sectors in each memory group is configurable;

a plurality of group tags, each of said group tags corresponds to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are erasable; and

a plurality of sector tags, each of said sector tags corresponds to a memory sector, each of said sector tags indicating whether the memory cells under the corresponding memory sector are erasable,

wherein all the memory cells belonging to one memory sector are erasable when either the corresponding sector tag or the corresponding group tag of the memory sector is set;

wherein any combination of memory sectors in a memory group can be simultaneously erased, and any combination of the memory groups can be simultaneously erased; and

wherein in response to too few tags being set, a received erase command is aborted.

Claims 34-41: Cancelled

42.(New) A memory system connectable to a plurality of hosts, comprising:

an interface for connection of the memory system to said hosts for the transfer of data and commands between the memory system and a host to which the system is connected;

a memory for storing said data, the memory section including:

a plurality of memory groups, each of said memory groups comprising a plurality of non-volatile memory cells;

write circuitry connectable to the memory cells to store data content therein; and

a plurality of group tags, each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells of the corresponding memory group are write protected;

a controller connected to the interface to receive the data and commands and to the memory to write and manage the storage of the data therein; and

registers connected to the controller to store information for the management of the memory, said information including a parameter indicating the size of the memory groups, wherein any combination of the memory groups can be write protected and said group tags are settable in response to a command from the host to which the memory system is connected.

43.(New) The memory system of claim 42, wherein the value of the parameter indicating the size of the memory groups is configurable by the host to which the card is connected.

44.(New) The memory system of claim 42, wherein said group tags are deselected in response to command from said host.

45.(New) The memory system of claim 42, wherein the memory is formed of a plurality of units of erase and the size of the groups is a plurality of the units of erase.

46.(New) The memory system of claim 42, wherein the memory is a flash memory.

47.(New) The memory system of claim 42, wherein the corresponding cells in each memory group are calculated in real time.

48.(New) A memory system connectable to a plurality of hosts, comprising:

an interface for connection of the memory system to said hosts for the transfer of data and commands between the memory system and a host to which the system is connected;

a memory for storing said data, the memory section including:

a plurality of memory groups, each of said memory groups comprising a plurality of memory sectors, each of said memory sectors comprising a plurality of non-volatile memory cells, wherein the number of memory sectors in each of the memory groups is configurable;

erase circuitry connectable to the memory cells for the erasure thereof;

a plurality of group tags, each of said group tags corresponds to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are erasable; and

a plurality of sector tags, each of said sector tags corresponds to a memory sector, each of said sector tags indicating whether the memory cells under the corresponding memory sector are erasable;

a controller connected to the interface to receive the data and commands and to the memory to manage the storage of the data therein; and

registers connected to the controller to store information for the management of the memory, said information including a parameter indicating number of memory sectors in each of the memory groups, wherein all the memory cells belonging to a given memory sector are erasable when either the corresponding sector tag or the corresponding group tag of the memory sector is set in response to a command from the host to which the memory system is connected, wherein all the memory cells belonging to a given memory sector are erasable by the erase circuitry when either the corresponding sector tag or the corresponding group tag of the memory sector is set, wherein any combination of memory sectors in each of said memory groups and any combination of the memory groups can be simultaneously erased.

49.(New) The memory system according to claim 48, wherein the corresponding sectors in each memory group is calculated in real time.

50.(New) The memory system according to claim 48, wherein said memory system is a flash memory.

51.(New) The memory system according to claim 48, wherein said ones of said sector tags and said group tags are deselectable in response to a command from the host to which the memory system is connected.

52.(New) The memory system according to claim 48, wherein the number of memory sectors in each memory group is configurable by a host to which the memory system is connected.